

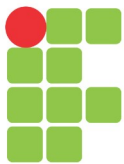
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CATARINENSE
Câmpus Luzerna

Sistemas Digitais

Introdução

Professor Ricardo Kerschbaumer
ricardo.kerschbaumer@ifc.edu.br

<http://professor.luzerna.ifc.edu.br/ricardo-kerschbaumer/>

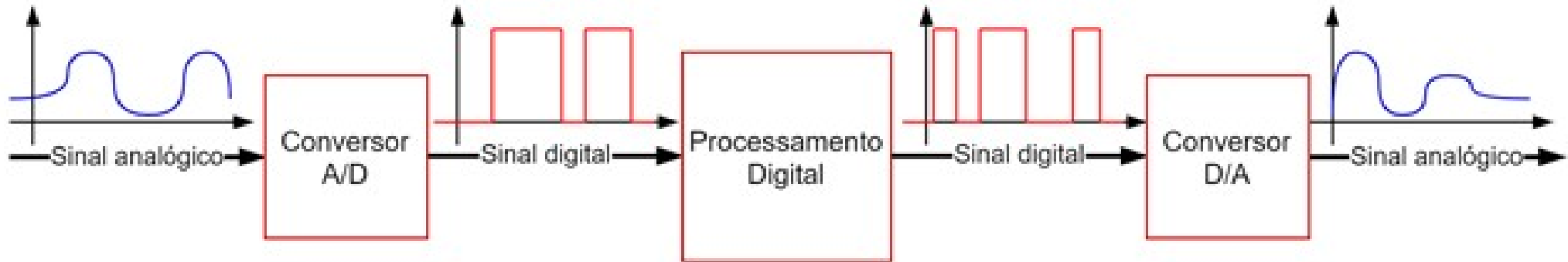
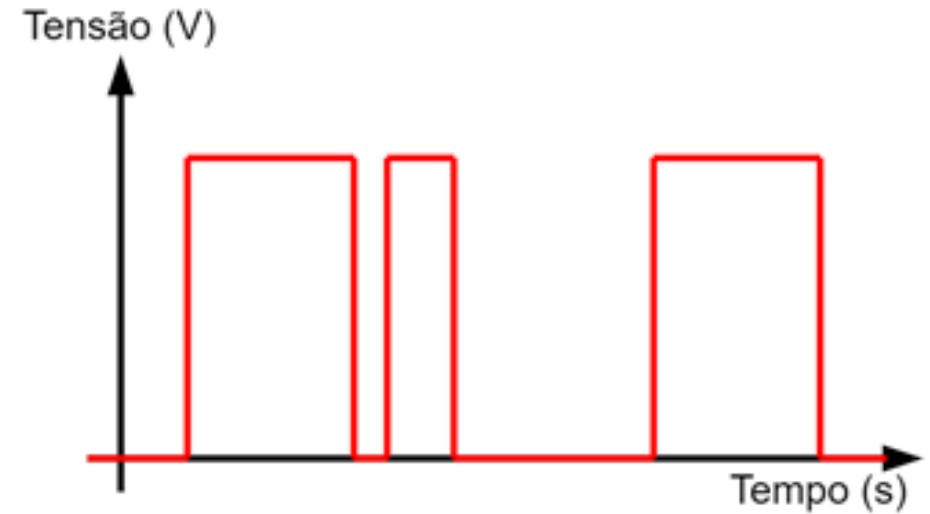
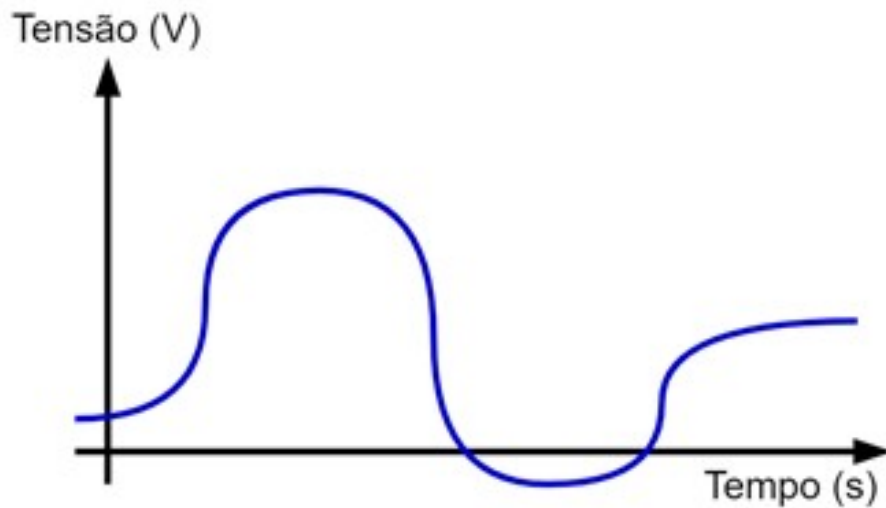


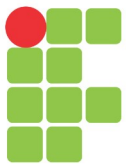
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Plano de Ensino

<http://professor.luzerna.ifc.edu.br/ricardo-kerschbaumer/>

Ementa: Conceitos introdutórios





Ementa: Códigos e sistemas numéricos

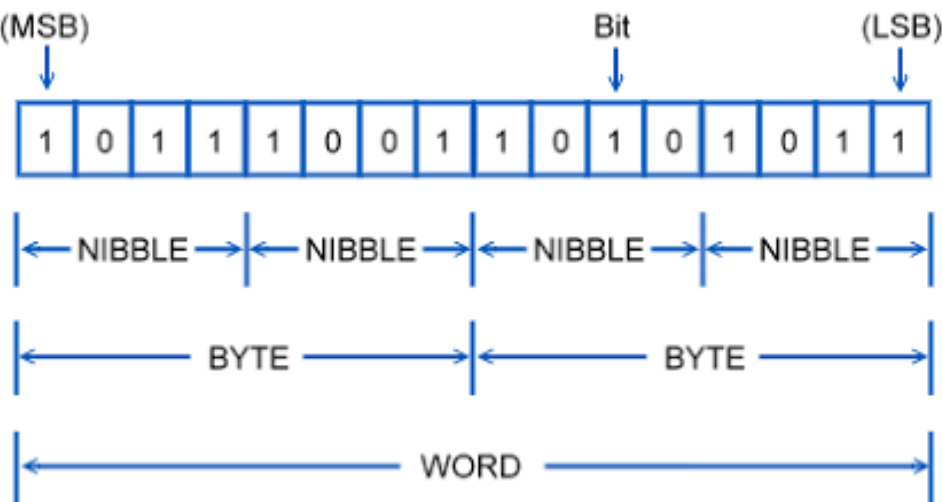
Decimal	BCD	Gray
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110

Decimal	BCD	Gray
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
128	64	32	16	8	4	2	1

42

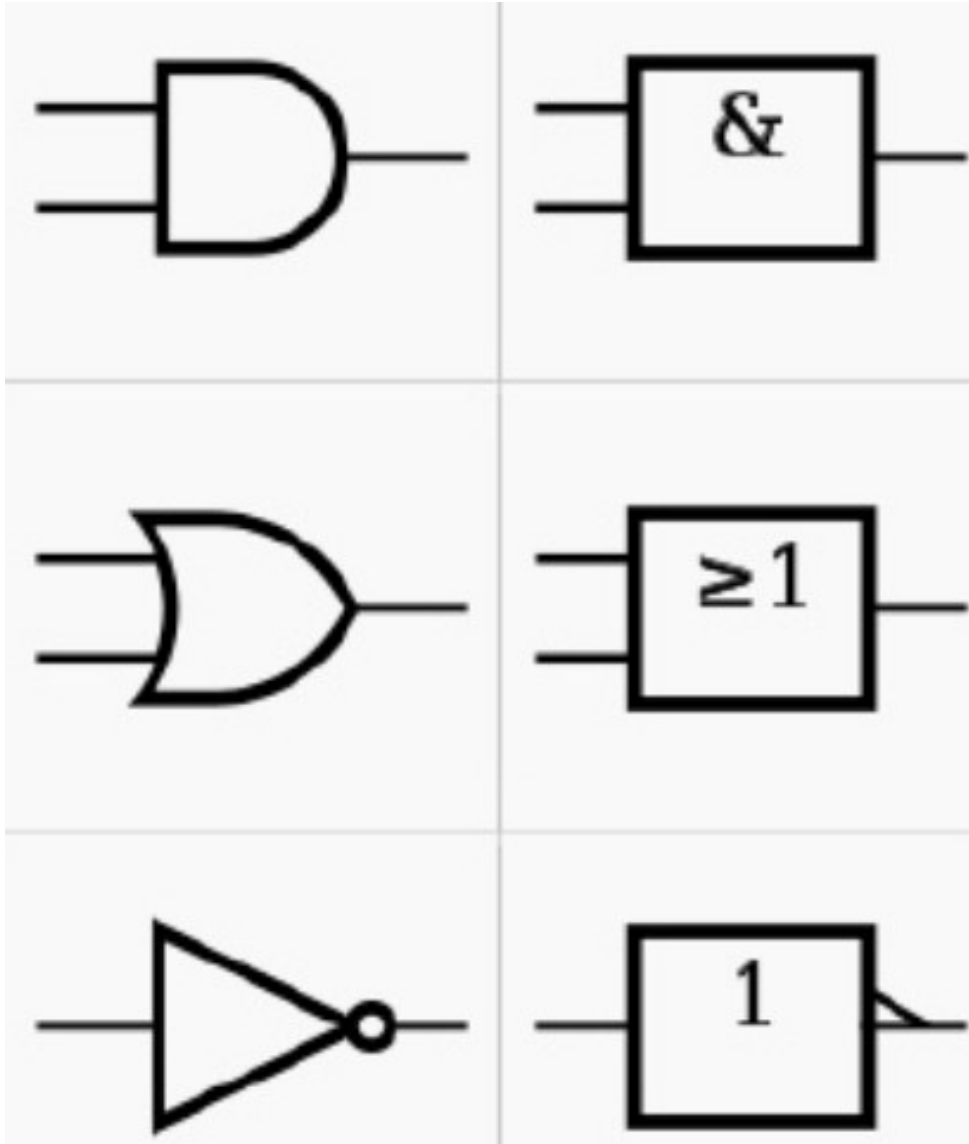
0	0	1	0	1	0	1	0
---	---	---	---	---	---	---	---



Decimal	Binary	ASCII	Decimal	Binary	ASCII	Decimal	Binary	ASCII	Decimal	Binary	ASCII
0	00000000	NUL	32	00100000	SP	64	01000000	@	96	01100000	`
1	00000001	SOH	33	00100001	!	65	01000001	A	97	01100001	a
2	00000010	STX	34	00100010	"	66	01000010	B	98	01100010	b
3	00000011	ETX	35	00100011	#	67	01000011	C	99	01100011	c
4	00000100	EOT	36	00100100	\$	68	01000100	D	100	01100100	d
5	00000101	ENQ	37	00100101	%	69	01000101	E	101	01100101	e
6	00000110	ACK	38	00100110	&	70	01000110	F	102	01100110	f
7	00000111	BEL	39	00100111	'	71	01000111	G	103	01100111	g
8	00001000	BS	40	00101000	(72	01001000	H	104	01101000	h
9	00001001	HT	41	00101001)	73	01001001	I	105	01101001	i
10	00001010	LF	42	00101010	*	74	01001010	J	106	01101010	j
11	00001011	VT	43	00101011	+	75	01001011	K	107	01101011	k
12	00001100	FF	44	00101100	,	76	01001100	L	108	01101100	l
13	00001101	CR	45	00101101	-	77	01001101	M	109	01101101	m
14	00001110	SO	46	00101110	.	78	01001110	N	110	01101110	n
15	00001111	SI	47	00101111	/	79	01001111	O	111	01101111	o
16	00010000	DLE	48	00110000	0	80	01010000	P	112	01110000	p
17	00010001	DC1	49	00110001	1	81	01010001	Q	113	01110001	q
18	00010010	DC2	50	00110010	2	82	01010010	R	114	01110010	r
19	00010011	DC3	51	00110011	3	83	01010011	S	115	01110011	s
20	00010100	DC4	52	00110100	4	84	01010100	T	116	01110100	t
21	00010101	NAK	53	00110101	5	85	01010101	U	117	01110101	u
22	00010110	SYN	54	00110110	6	86	01010110	V	118	01110110	v
23	00010111	ETB	55	00110111	7	87	01010111	W	119	01110111	w
24	00011000	CAN	56	00111000	8	88	01011000	X	120	01111000	x
25	00011001	EM	57	00111001	9	89	01011001	Y	121	01111001	y
26	00011010	SUB	58	00111010	:	90	01011010	Z	122	01111010	z
27	00011011	ESC	59	00111011	;	91	01011011	[123	01111011	{
28	00011100	FS	60	00111100	<	92	01011100	\	124	01111100	
29	00011101	GS	61	00111101	=	93	01011101]	125	01111101	}
30	00011110	RS	62	00111110	>	94	01011110	^	126	01111110	~
31	00011111	US	63	00111111	?	95	01011111	_	127	01111111	DEL

Ementa:

Portas lógicas e álgebra booleana



Porta
"E"

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Porta
"OU"

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

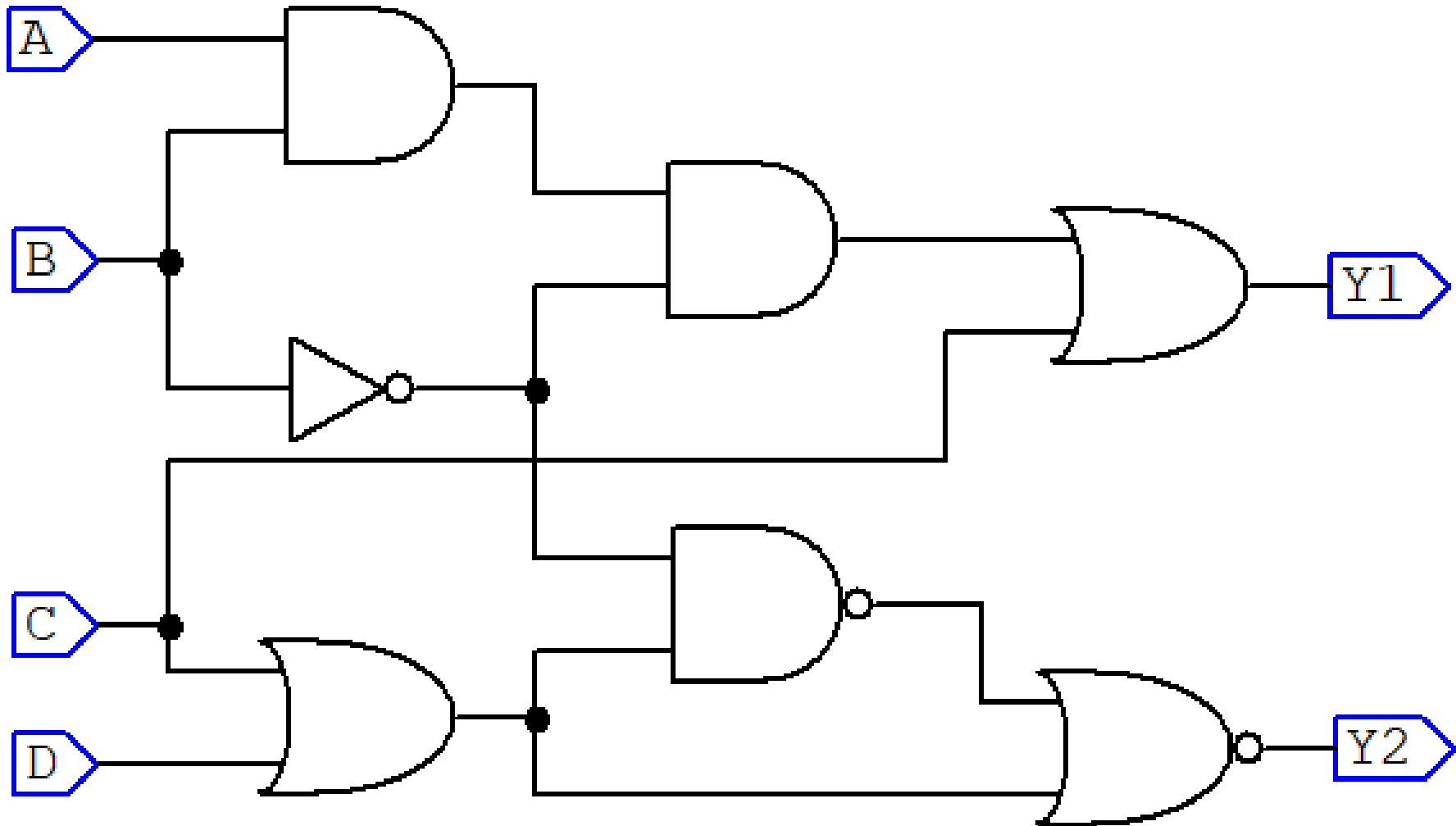
Porta
"Inversora"

A	Y
0	1
1	0

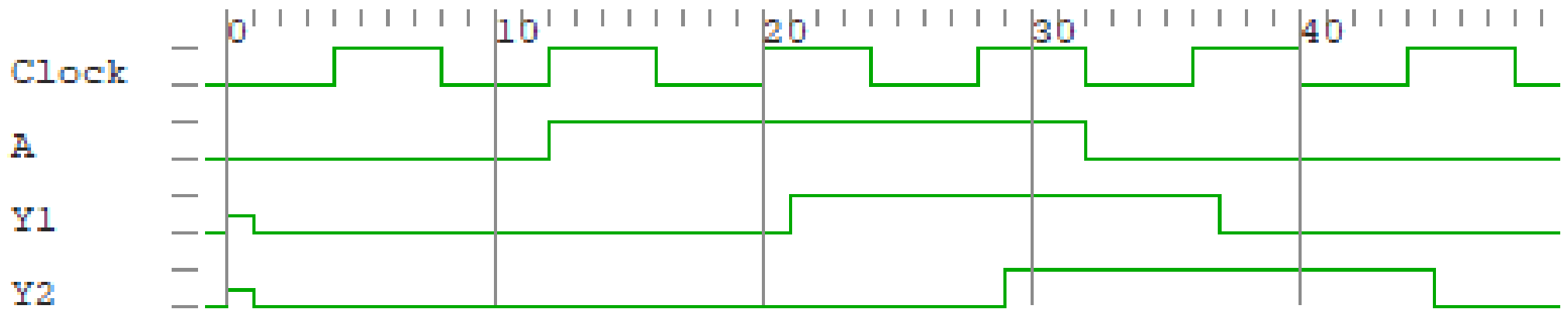
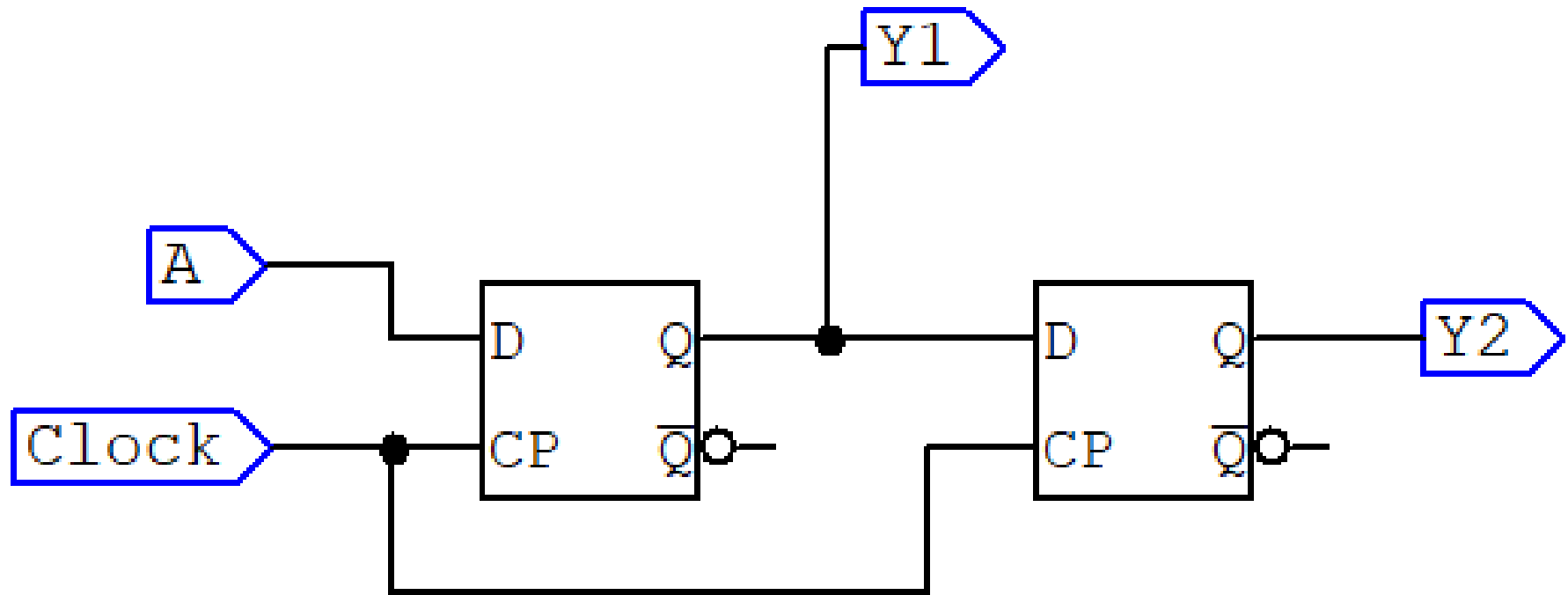
$$\overline{XY} = \overline{X} + \overline{Y}$$

$$\overline{X + Y} = \overline{X} \overline{Y}$$

Ementa: Circuitos lógicos combinacionais

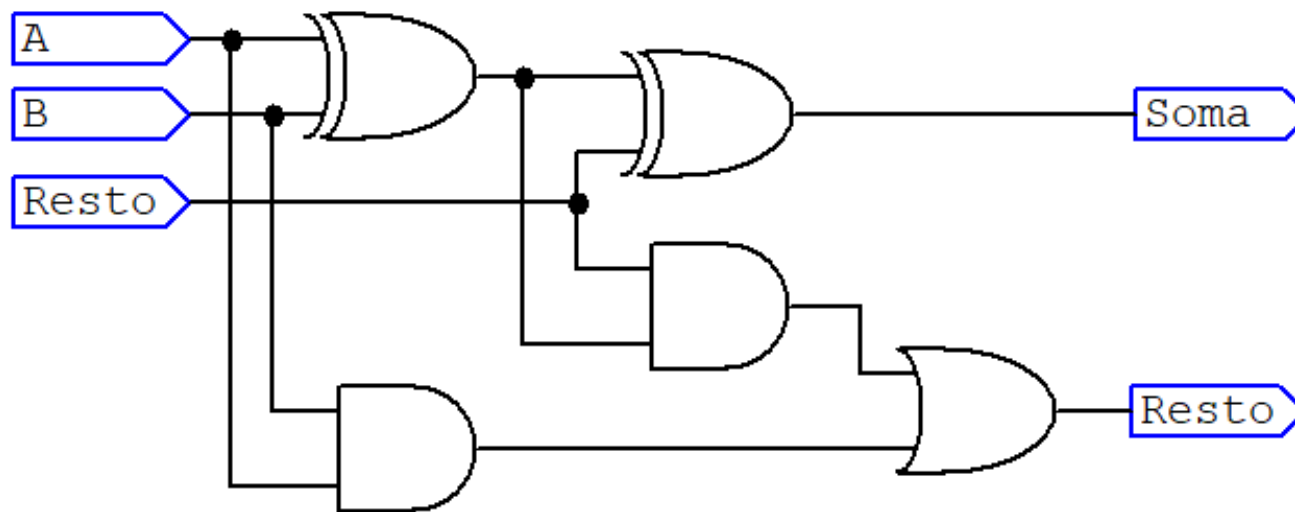


Ementa: Circuitos lógicos sequenciais



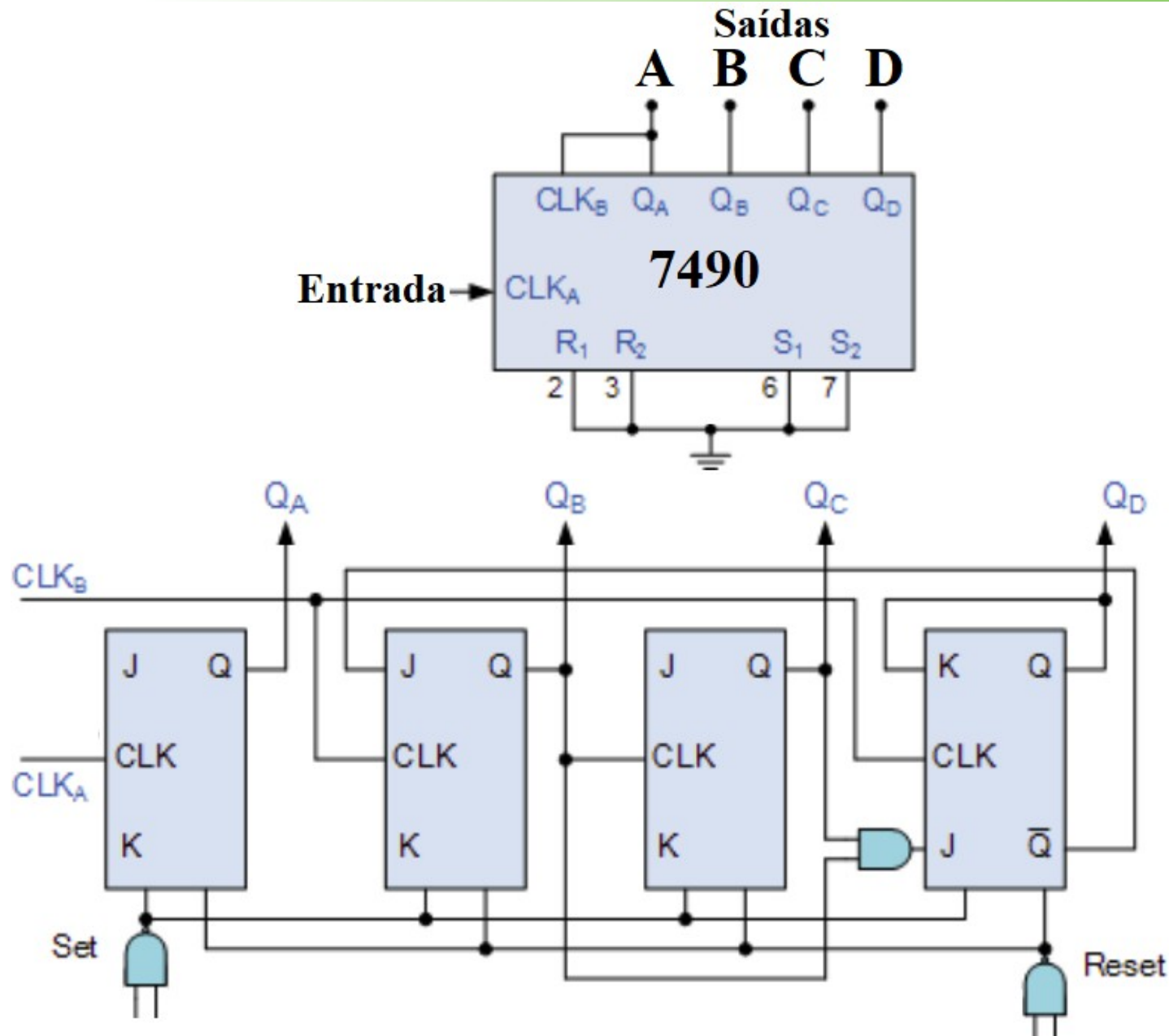
Ementa: Aritmética digital

Exemplo de Somador



Entradas			Saídas	
A	B	R	S	R
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Ementa: Contadores e registradores



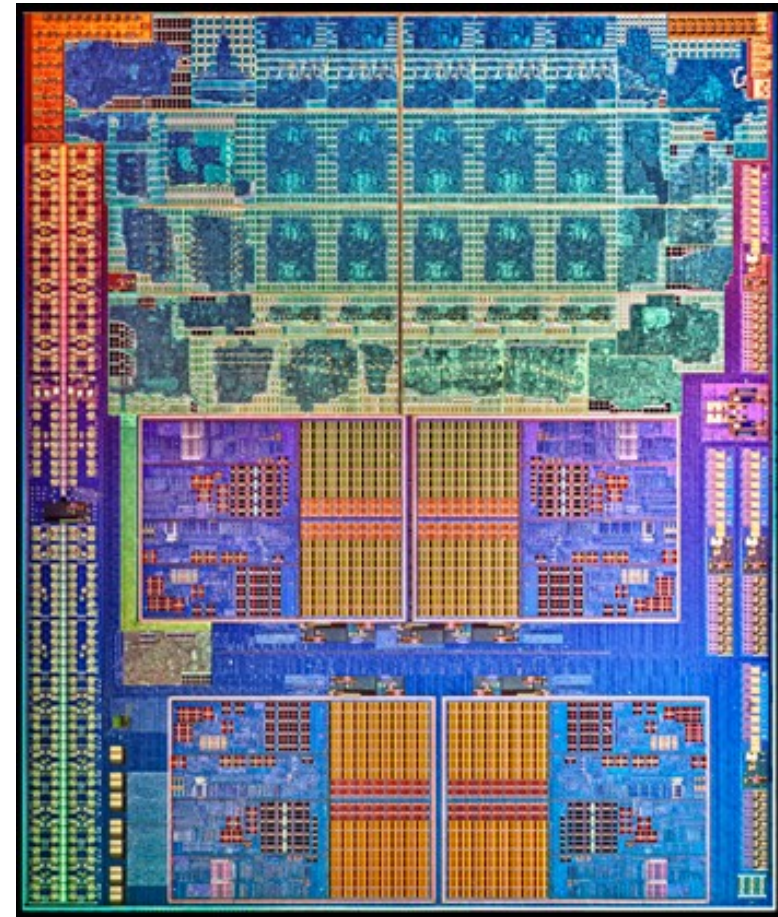
Ementa: Famílias lógicas

Famílias Lógicas Atuais

- CMOS (Complementary Mosfet)
- TTL (Transistor-Transistor Logic)

Famílias Lógicas Obsoletas

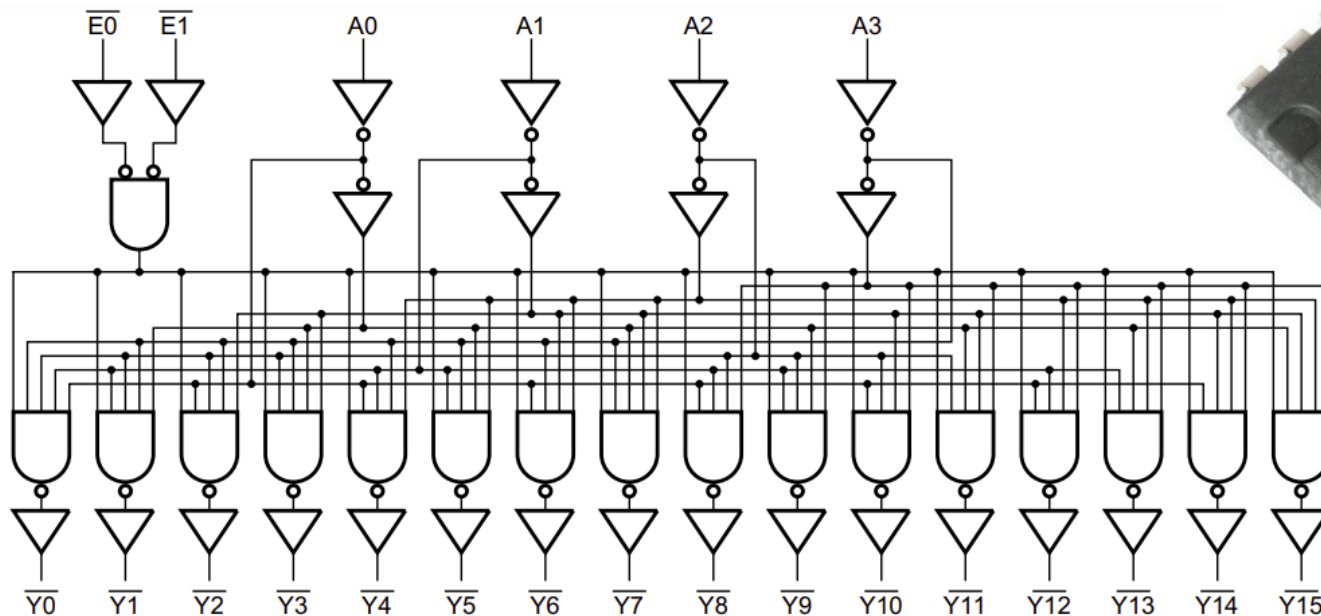
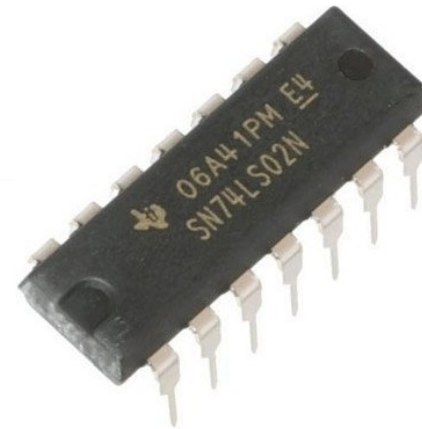
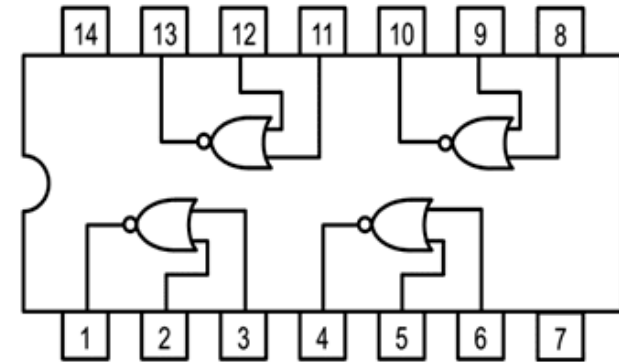
- DCTL (Direct-Coupled Transistor Logic)
- RTL (Resistor-Transistor Logic)
- RCTL (Resistor-Capacitor Transistor Logic)
- DTL (Diode-Transistor Logic)
- HTL (High-Threshold Logic)
- ECL (Emitter-Coupled Logic)

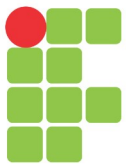


Ementa:

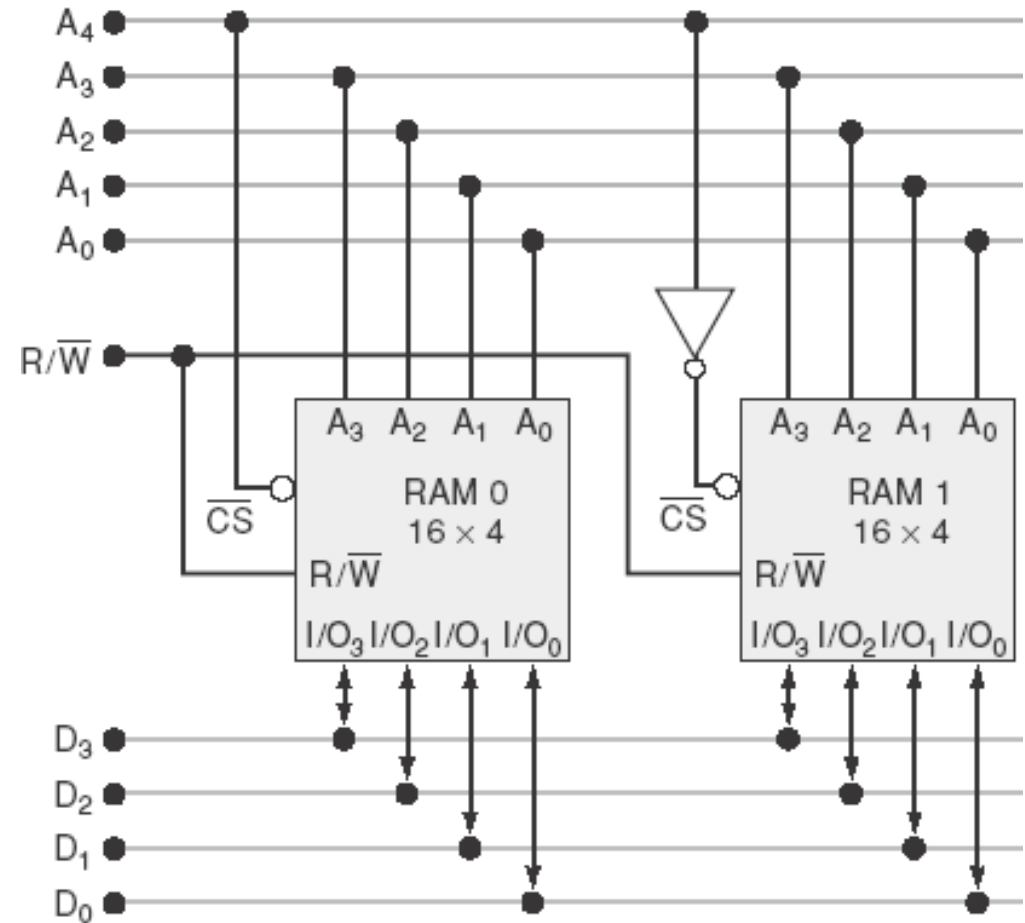
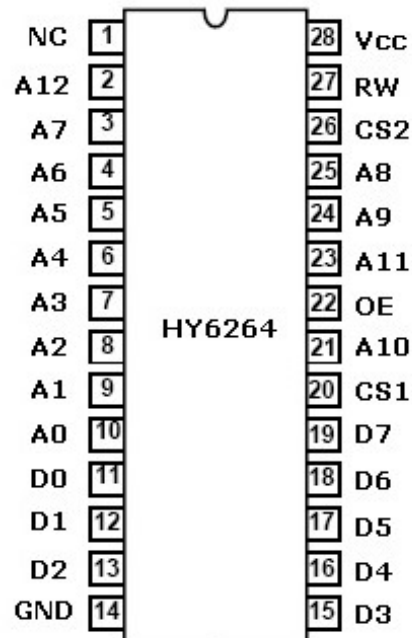
Circuitos lógicos MSI

(Medium Scale Integration)

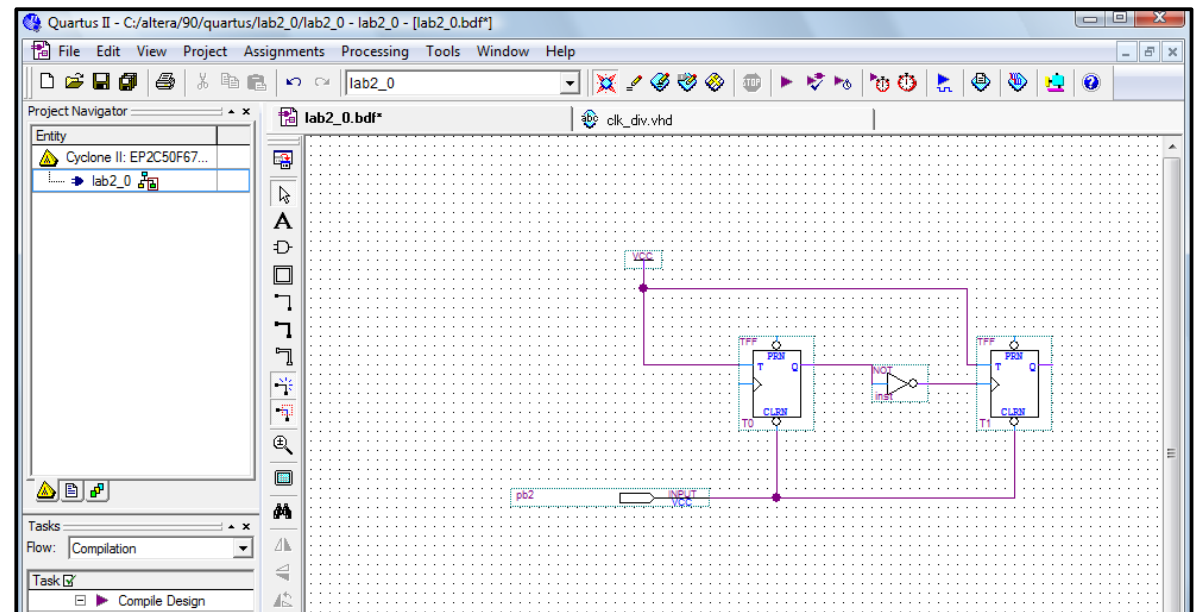
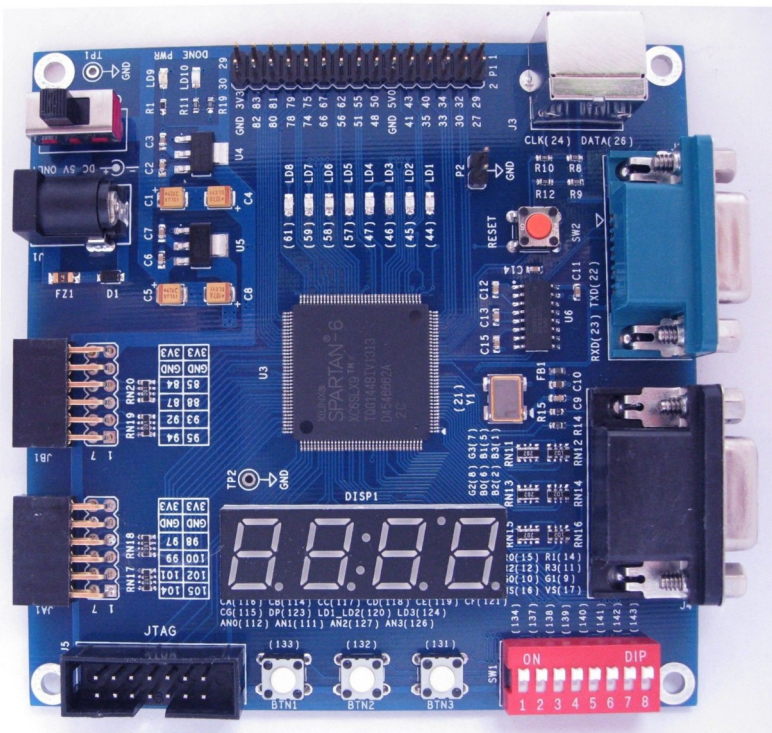
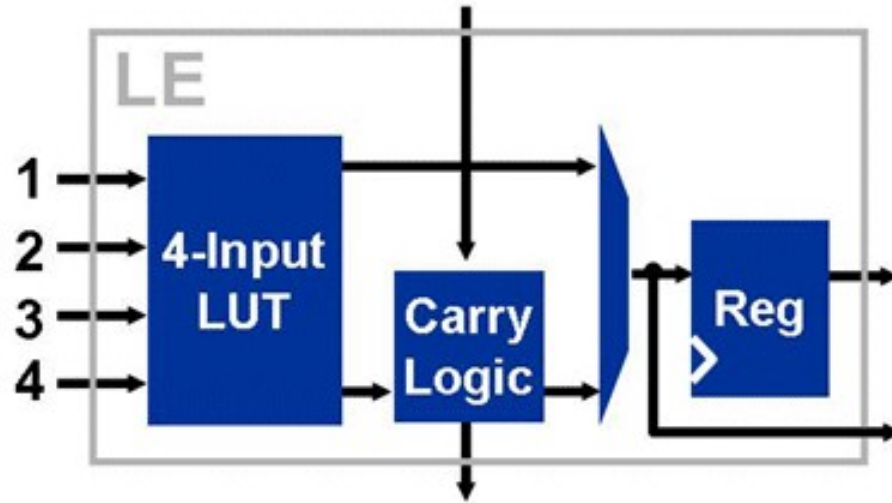


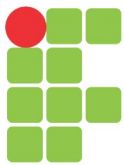


Ementa: Memórias



Ementa: Dispositivos lógicos programáveis





Simulações

Hneemann Digital - <https://github.com/hneemann/Digital>

